

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Attorney Docket Number	40704/PYI/F179
Application Number	09/851,708
Filing Date	May 8, 2001
Applicant(s)	Indradeep Ghosh
Group Art Unit	
Examiner Name	Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
R50	5,513,123	04/1996	Dey et al.	364	489	
R50	5,602,856	02/1997	Teramoto	371	27	
R50	5,615,124	03/1997	Hemmi et al.	364	488	
R50	5,625,630	04/1997	Abramovici et al.	371	22.1	
R50	5,696,771	12/1997	Beausang et al.	371	22.3	
R50	5,875,196	02/1999	Chakradhar et al.	371	22.1	
R50	5,883,809	03/1999	Sullivan et al.	364	489	
R50	5,933,356	08/1999	Rostoker et al.	364	489	
R50	5,991,523	11/1999	Williams et al.	395	500.19	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

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R50	SANDHYA SESHADRI and MICHAEL S. HSIAO, "An Integrated Approach to Behavioral-Level Design-For-Testability Using Value-Range and Variable Testability Techniques", International Test Conference, 1999, pp. 858-867.
R50	ALBRECHT P. STROELE, "Synthesis for Arithmetic Built-In Self-Test", 18 th IEEE VLSI Test Symposium, Montreal, Canada, May 2000, pp. 165-170.
R50	ALBRECHT P. STROELE, "Synthesizing Data Paths with Arithmetic Self-Test", IEEE International Symposium on Circuits and Systems (ISCAS), Geneva, Switzerland, May 2000, pp. II-45-48.
R50	MARK C. HANSEN and JOHN P. HAYES, "High-Level Test Generation using Physically-Induced Faults", VLSI Test Symposium Paper, May 1995, pp. 1-9.

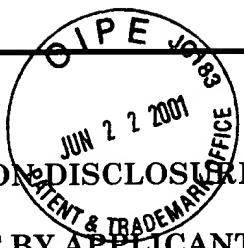
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FORM PTO-1449

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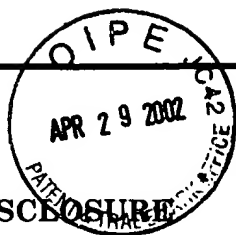
OTHER DOCUMENTS

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<i>RSO</i>	JAAN RAIK, "Hierarchical Test Generation Based on Alternative Graph Models", Computer Engineering and Diagnostics Department of the Institute of Computer Engineering, April 1997, pp. 1-44, Tallinn Technical University, Estonia.
<i>RSO</i>	INDRADEEP GHOSH, ANAND RAGHUNATHAN and NIRAJ K. JHA, "Design for Hierarchical Testability of RTL Circuits Obtained by Behavioral Synthesis", IEEE International Conference on Computer Design, 1995, pp. 1-27.
<i>RSO</i>	INDRADEEP GHOSH, ANAND RAGHUNATHAN, and NIRAJ K. JHA, "A Design for Testability Technique for RTL Circuits Using Control/Data Flow Extraction", In Proc. IEEE International Conference on Computer-Aided Design, 1996.
<i>RSO</i>	INDRADEEP GHOSH, ANAND RAGHUNATHAN, and NIRAJ K. JHA, "Hierarchical Test Generation and Design for Testability of ASPPs and ASIPs", ACM, Inc., DAC 97, Anaheim, California.
<i>RSO</i>	SILVIA CHIUSANO, FULVIO CORNO, PAOLO PRINETTO, "RT-level TPG Exploiting High-Level Synthesis Information, 17 th IEEE VLSI Test Symposium, April 1999.
<i>RSO</i>	YIORGOS MAKRIS and ALEX ORAILOGLU, "Property-Based Testability Analysis for Hierarchical RTL Designs", In Proceedings of the IEEE International Conference on Electronics Circuits and Systems, pp. 1089-1092, 1999.
<i>RSO</i>	INDRADEEP GHOSH, NIRAJ K. JHA and SUDIPTA BHAWMIK, "A BIST Scheme for RTL Circuits Based on Symbolic Testability Analysis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, January 2000.

EXAMINER SIGNATURE	<i>R. Stephen D. Dine</i>	DATE CONSIDERED	<i>1/23/2004</i>
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Attorney Docket Number	40704/DMC/F179
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Filing Date	May 8, 2001
Applicant(s)	Indradeep Ghosh
Group Art Unit	2858
Examiner Name	To Be Assigned

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD		Farzan FALLAH, et al., "Simulation Vector Generation from HDL Descriptions for Observability-Enhanced Statement Coverage", 36 th Design Automation Conference, New Orleans, 6 pgs, (June 1999)
RSD		Abhijit GHOSH, et al., "Sequential Test Generation and Synthesis for Testability at the Register-Transfer and Logic Levels", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 5, pp 579-598 (May 1993)

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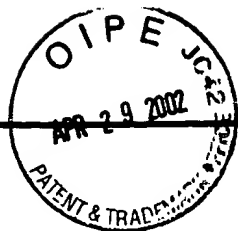
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RSD		Viraphol CHAIYAKUL, et al., "High-Level Transformations for Minimizing Syntactic Variances", 30 th ACM/IEEE Design Automation Conference, pp 413-418 (1993)
RSD		Fulvio CORNO, et al., "Testability Analysis and ATPG on Behavioral RT-Level VHDL", IEEE, International Test Conference, Paper 30.4, pp 753-759 (1997)
RSD		Sujit DEY, et al., "Non-Scan Design-For-Testability of RT-Level Data Paths", ACM, 11 pages (1994)

EXAMINER SIGNATURE	<i>R. S. Ghosh</i>	DATE CONSIDERED	1/23/2004
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<i>RSO</i>		LAMPORT, L., "The Temporal Logic of Actions", Revised Version of SRC Research Report 79 to appear in ACM Transactions on Programming Languages and Systems, (19 pages) April 1994.
<i>RSO</i>		GHOSH, S., "Test Compaction at the Register Transfer or Behavior level", Project Report, ELE 466: Digital System Testing, Dept. of Electrical Engineering, Princeton University, Princeton, NJ (8 pgs), 1994.
<i>RSO</i>		K. Chakrabarty, R. Mukherjee and A. Exnicios, "Synthesis of Transparent Circuits for Hierarchical and System-on-a-Chip Test", Proc. IEEE International Conference on VLSI Design, pp. 431-436, Bangalore, India, January 2001.

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